IN THE DRAWINGS

Applicants enclose an "Annotated Mark-up Drawings" and a "Replacement Sheet" for Fig. 14, adding reference numeral 307 to be consistent with the disclosure in the specification.

REMARKS

Claims 15-46 have been canceled. Claims 1-14 and 47 remain pending in the present application. Pursuant to 37 CFR § 1.173(b) and (d), Applicants submit all changes to the patent being reissued, including all changes made to the specification, Fig. 14, and the claims throughout this reissue application. Applicants refer to Figs. 1-6 and their corresponding description in the specification for illustrative embodiments of newly-added generic claim 47. Claims 1-14 were amended to be consistent with newly-added generic claim 47. In response to the final Office Action, Applicants amended the specification and claims 1, 2, 5, 8, and 14 to correct minor errors and to properly claim the subject matter of the invention. No new matter has been added.

REJECTION UNDER 35 U.S.C. § 251

Claims 1 – 14 and 47 stand rejected under 35 U.S.C. § 251 for a defective Reissue Oath or Declaration that failed to comply with 37 CFR § 1.175. In accordance with 37 CFR § 1.175, Applicants enclose a Reissue Application Declaration By The Inventor, signed by Applicants, declaring that:

1. Applicants believe the original patent to be partly inoperative or invalid by reason of a defective specification or drawing;

2. Applicants believe the original patent to be partly inoperative or invalid by reason of the patentees claiming less than patentees had the right to claim in the patent

3. Applicants believe the original patent to be partly inoperative or invalid by reason of other errors; and

4. each and every error corrected in the present Reissue application arose without any deceptive intention on the part of Applicants.

Further in accordance with 37 CFR § 1.175(a)(1), Applicants specify at least the error being relied upon as the bases for a broadening reissue in the signed Declaration—namely, that a generic claim encompassing the elected species covered by the claims of the issued patent and one or more non-elected species was mistakenly omitted during the prosecution of the issued patent, thus rendering the issued patent "partly inoperative or invalid by reason of the patentees claiming less than patentees had the right to claim in the patent." Accordingly, Applicants declare that newly-added claim 47 is submitted with the present reissue to correct this error.

The Federal Circuit Court of Appeals has permitted a patentee to file a reissue application to present a so-called linking claim, a claim broad enough to read on or link the invention elected (and patented) together with the invention not elected. In re Doyle, 293. F.3d 1355, U.S.P.Q.2d 1161 (Fed. Cir. 2002). Applicants respectfully submit that newly-added claim 47 is such a linking claim that encompasses both the elected group of the issued claims 1-14 and one or more non-elected species described in the specification.

For instance,

> "(i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal..." (emphasis added)

recited in claim 47 includes the elected group covered by claims 1-14 (e.g., "between input and output signals of said equalizing circuit" recited in claim 1), which the Examiner identified as a species illustrated by Fig. 1 and its corresponding description in the specification. Applicants respectfully submit that the above-cited recitation of claim 47 is generic to the elected species and at least two non-elected species, which were identified by the Examiner to be illustrated by Figs. 2 and 3, respectively. Applicants further submit that the phrase,

> "(ii) a combination of clock phase difference information to be supplied to said identifying circuit and signal error differential

> information obtained by said identifying circuit, and then supplying said phase component to said clock regenerating circuit,"

recited in claim 47 encompasses at least the remaining non-elected species identified by the Examiner, which are illustrated by Figs. 4-6, respectively.

In view of the foregoing reasons, Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C. § 251 for a defective reissue declaration.

OBJECTION TO SPECIFICATION, CLAIMS

The specification is objected to at column 14, line 1 in regard to informalities. Claims 1, 2, 5, 8, 11 and 47 are also objected to in regard to informalities. Applicants thank the Examiner for suggesting amendments to the specification and these claims in order to overcome this rejection, and amend the specification and claims 1, 2, 5, 8, 11 and 47 in accordance with these suggestions. Applicants therefore respectfully request that the objection to the specification and to claims 1, 2, 5, 8, 11 and 47 be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 102

Claim 47 is rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,317,602 to Onoda et al. Claim 47 is also rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,535,252 to Kobayashi. Applicants respectfully traverse these rejections.

Claim 47 recites the following:

> "A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:
>
> an identifying circuit for identifying a demodulated signal at a predetermined identification level, said demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal;
>
> a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit; and

a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including any one of (i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to said identifying circuit and signal error differential information obtained by said identifying circuit, and then supplying said phase component to said clock regenerating circuit,

said clock phase detecting section including

a difference detecting unit, responsive to the receipt of said composite input information, for detecting any one of (I) difference information between the demodulated signal and the equalized demodulated signal and (II) a combination of the clock phase difference information and the signal error differential information, and

a clock phase calculating unit for calculating said phase component of said signal identification clock based on the output from said difference detecting unit."

Significantly, independent claim 47 recites as a necessary component a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including any one of (i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to said identifying circuit and signal error differential information obtained by said identifying circuit.

Onoda discloses a QPSK base-band delayed detector (see, e.g., FIG. 5 of Onoda). The detector of Onoda includes A/D converters 57, 58 for identifying and converting analog signals into digital signals and bit timing recovery (BTR) circuit 1 including phase comparison result detection unit 2 for detecting a phase component of the digital signals generated by converter 57, 58, and a digital PLL 3 for outputting a clock signal of appropriate phase. Unlike Applicants' claimed invention, however, Onoda fails to disclose that detection unit 2 detects either of a)

difference information between the demodulated signal and the equalized demodulated signal, or b) a combination of clock phase difference information and signal error differential information.

Onoda nowhere discloses means to produce an equalized signal (for example, by means of an equalizing circuit), and therefore fails to disclose a detection unit that detects Applicants' claimed difference information between the demodulated signal and the equalized demodulated signal. In addition, Onoda fails to disclose a detection unit that detects Applicants' claimed combination of clock phase difference information and signal error differential information.

With reference to FIG. 5 of Onoda, Onoda discloses that I-channel data I' (a) moves from operation circuit 59 to flip flop (FF) 21, and that Q-channel data Q' moves from operation circuit 59 to FF 22. FF 21 samples a most significant bit (MSB) of the I-channel data I' (a) in synchrony with a data sampling clock signal (d) obtained from divider 34 (see, e.g., column 5, lines 54 – 61 of Onoda). As this MSB is not an error bit, the I-channel data I' (a) fails to correspond to signal error information, as is required by the present invention.

In addition, and again with reference to FIG. 5 of Onoda, the output of the divider 34 is data detecting a clock signal supplied to discriminators 60, 61 and parallel to serial converter (P/S) 62, and is not data detecting a clock signal supplied to analog to digital converters (A/Ds) 57, 58. As a result, while the detected clock signal may have clock phase information, it cannot have clock phase difference information, as is required by the present invention.

Kobayashi discloses a DQPSK clock synchronization circuit (see, e.g., FIG. 2 of Kobayashi). The circuit of Kobayashi includes A/D converters 41, 42 for detecting and converting analog signals into digital signals, phase detector error circuit 47 for detecting a phase error in the digital signals, and clock reproducer 48 for generating a clock signal m for A/D converters 41, 42. As in the case of Onoda, and in sharp contrast to Applicants' claimed

invention, however, Kobayashi fails to disclose that detector circuit 47 detects either of a) difference information between the demodulated signal and the equalized demodulated signal, or b) a combination of clock phase difference information and signal error differential information.

Kobayashi nowhere discloses means to produce an equalized signal (for example, using an equalizing circuit), and therefore fails to disclose a detection unit that detects Applicants' claimed difference information between the demodulated signal and the equalized demodulated signal. In addition, Kobayashi fails to disclose a detection unit that detects Applicants' claimed combination of clock phase difference information and signal error differential information.

With reference to FIG. 2 of Kobayashi, Kobayashi discloses that a judgment timing clock signal l is supplied from the clock reproducer 48 to a judger 44 and the phase error detector 47. However, this judgment timing clock signal is not supplied to A/Ds 41, 42. The phase error detector 47 extracts judgment timing (a BTR pattern) from its outputs by means of a filter output I from band pass filter 46, and detects a phase error j with respect to a current judgment timing clock signal l (see, e.g., column 6, lines 57 – 61 of Kobayashi). As a result, the phase error detector 47 fails to detect clock phase difference information, as is required by the present invention.

Accordingly, Applicants respectfully submit that claim 47 is not anticipated by either of Onoda and Kobayashi, and is therefore allowable.

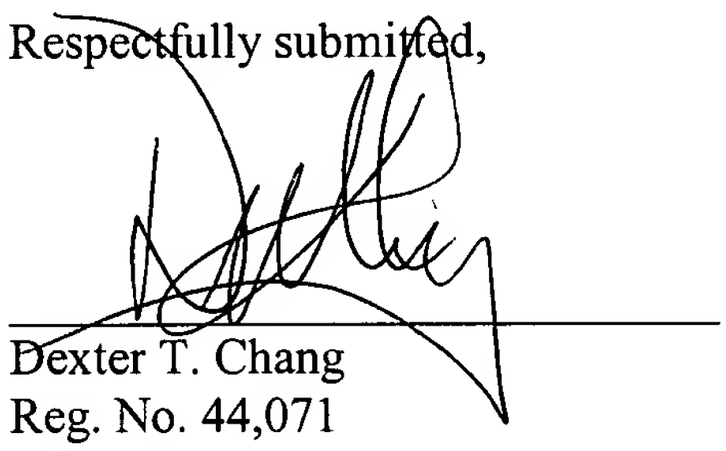
The above statements on the disclosures in the cited references represent the present opinions of the undersigned attorney. The Examiner is respectfully requested to specifically indicate those portions of the respective reference that provide the basis for a view contrary to any of the above-stated opinions.

Applicants appreciate the Examiner's implicit finding that the additional U.S. patents made of record, but not applied, do not render the claims of the present application unpatentable, whether these references are considered alone or in combination with others.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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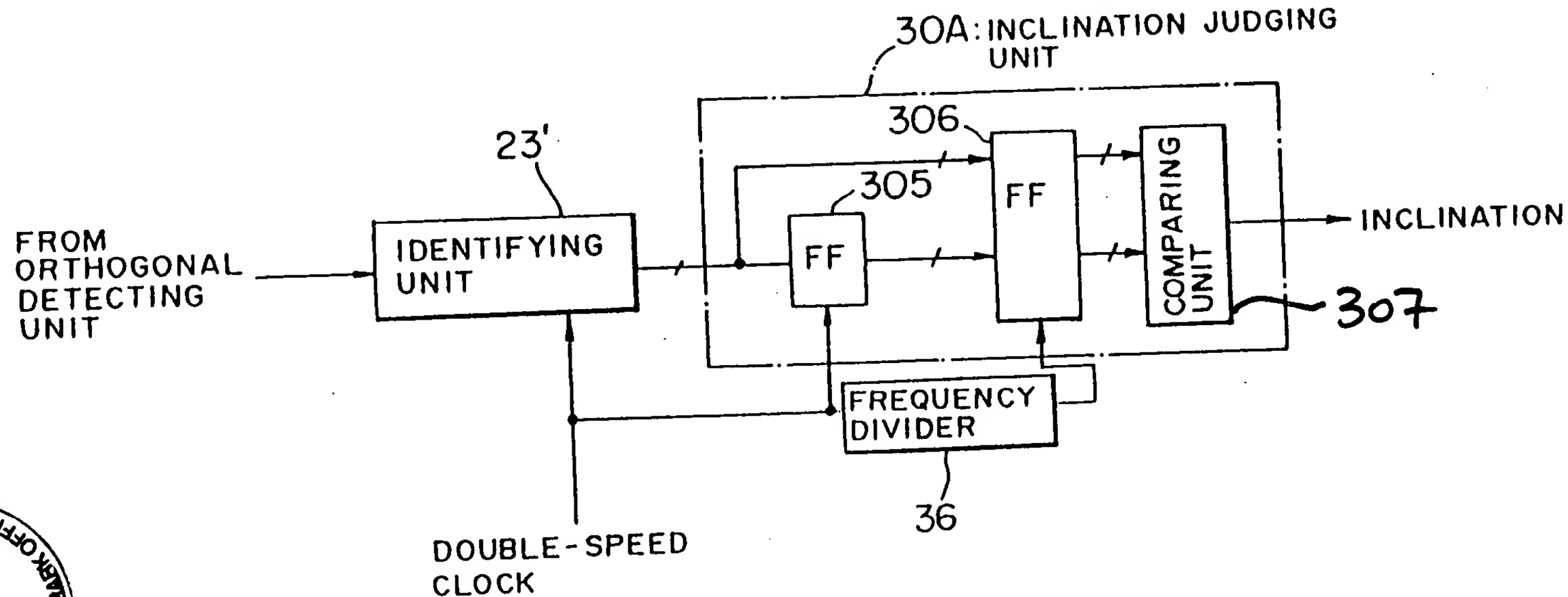
Amended

FIG. 14



Annotated Mark-up Drawings